

FIG. 1

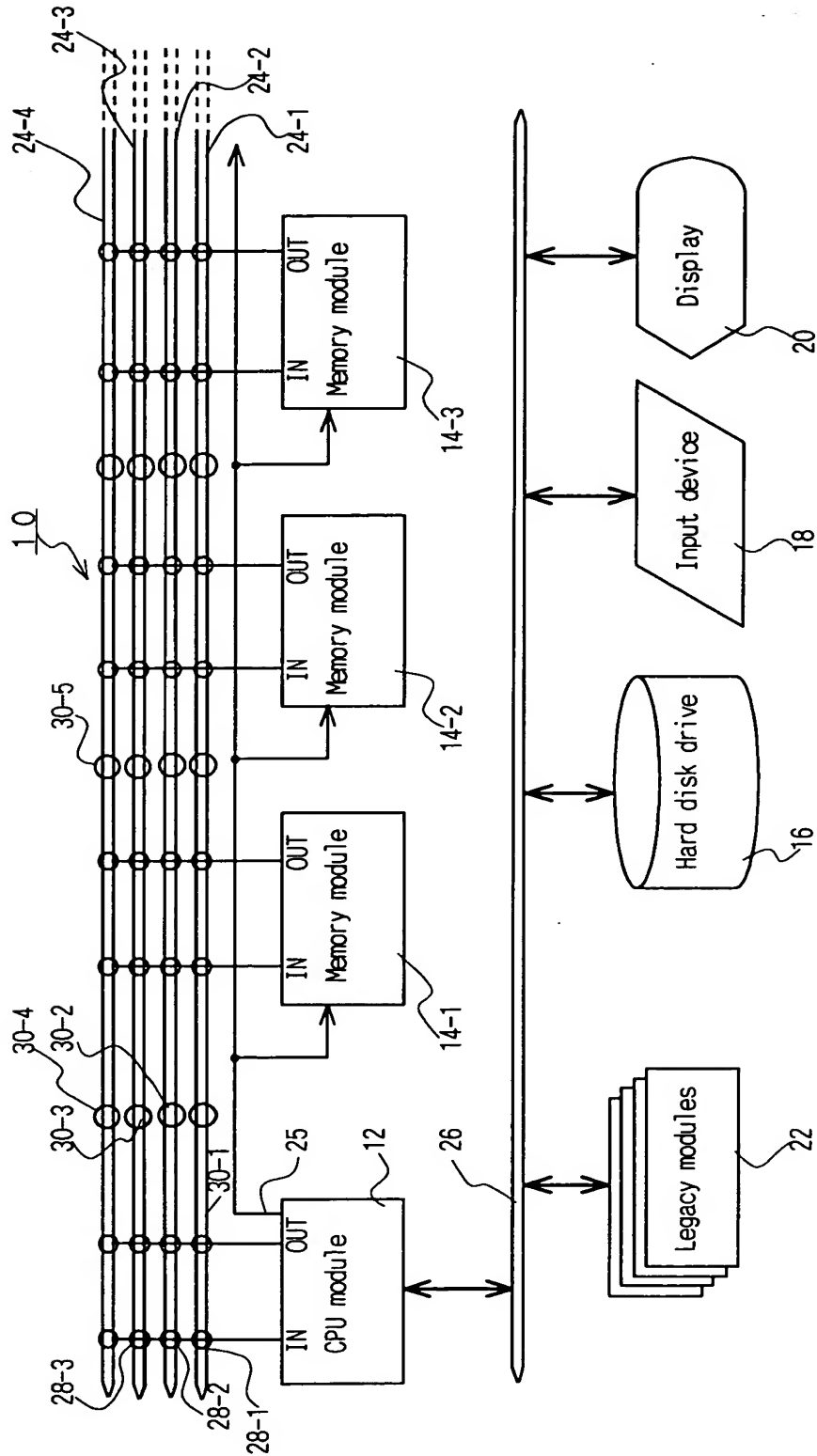


FIG. 2

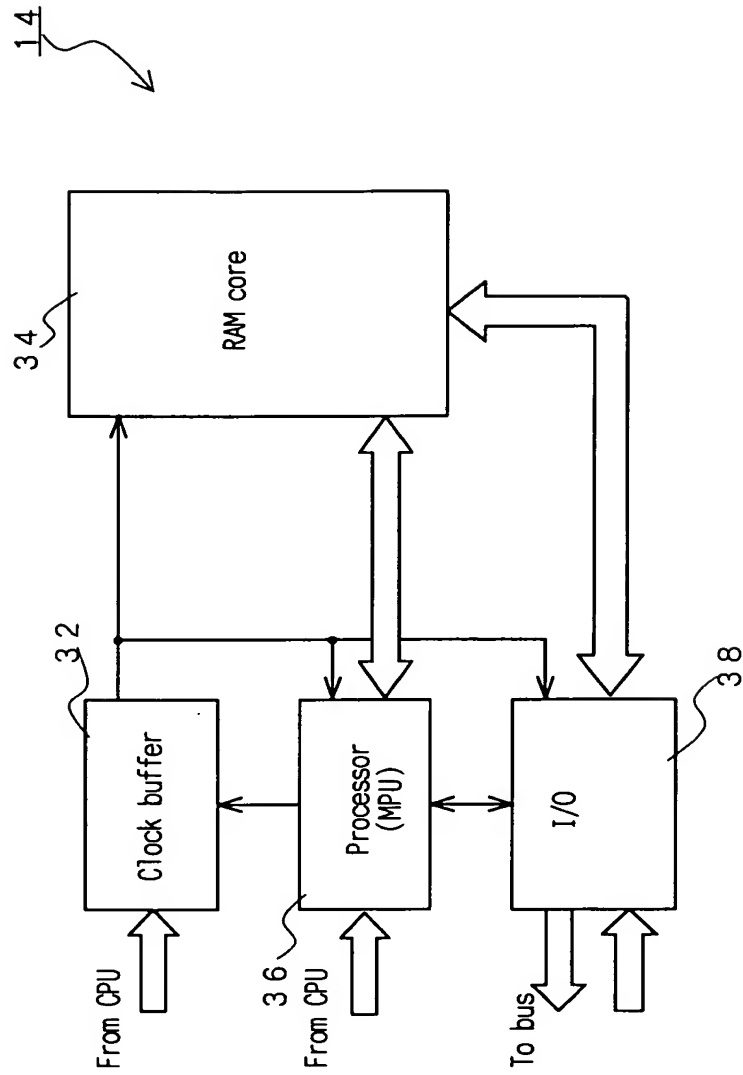


FIG. 3

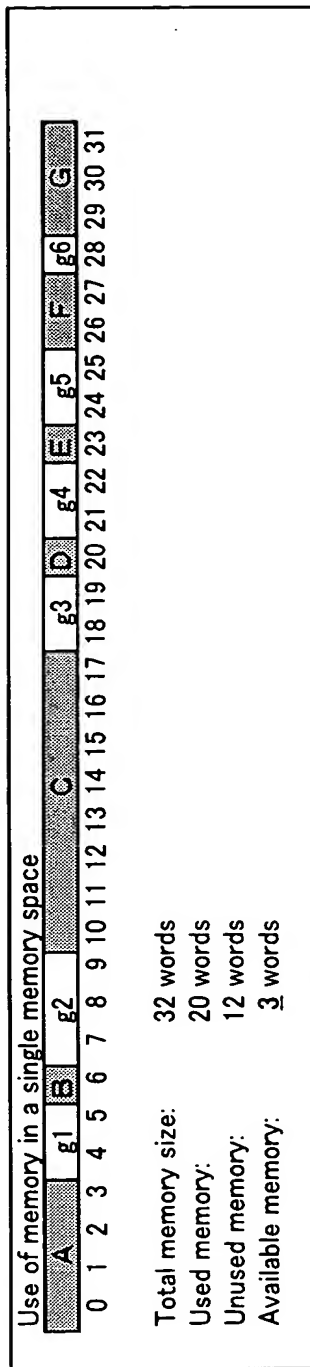
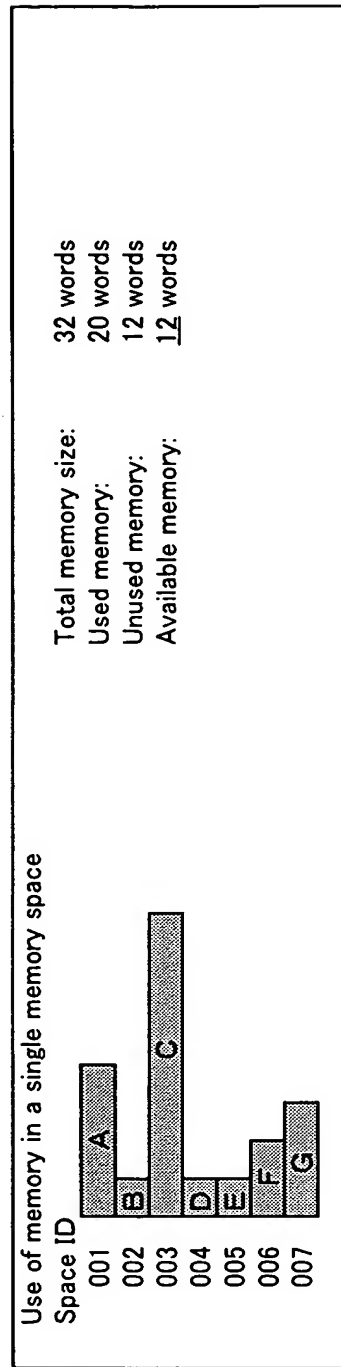


FIG. 4



4/23

FIG. 5

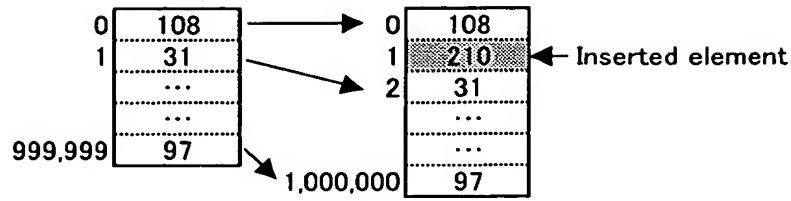


FIG. 6

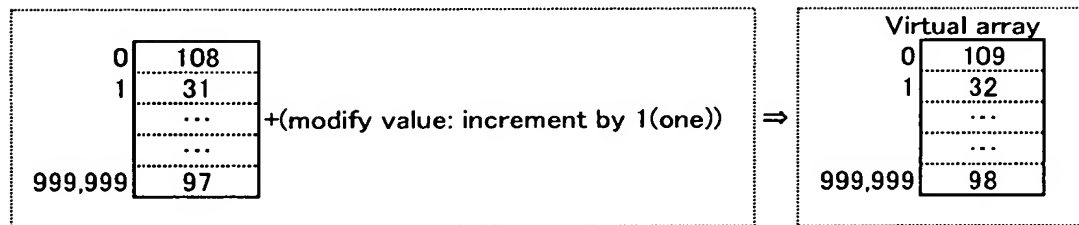


FIG. 7

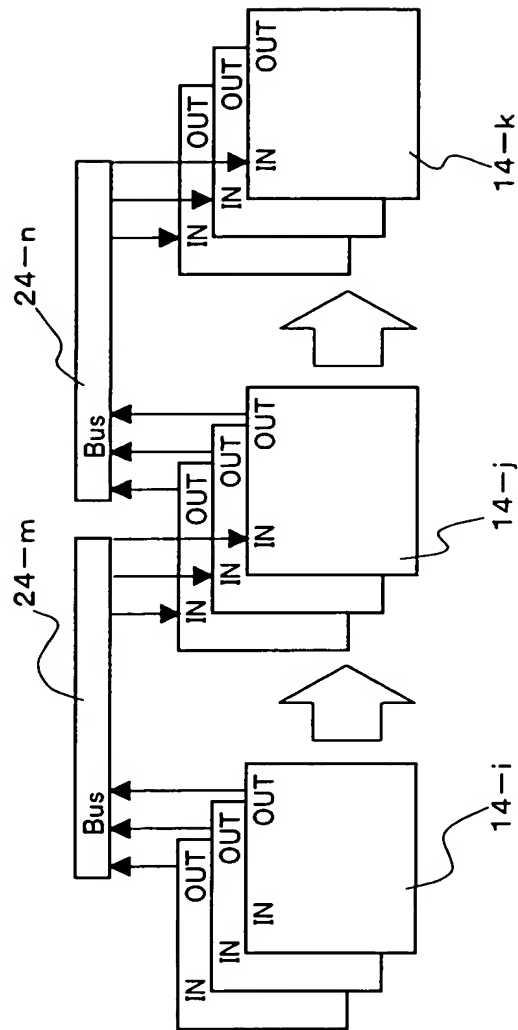


FIG. 8A

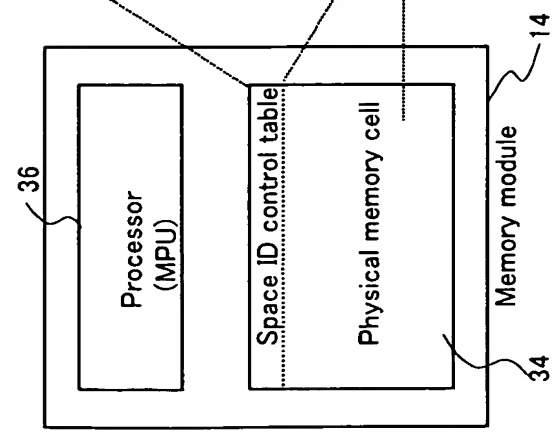


FIG. 8B

Logical Allocated On-chip			Access	
Space ID	start address	region size	physical address	control flags
010	100	60	0	R
010	160	4	80	R
016	0	20	60	RW
...	...	...	...	...
...	...	...	...	...
212	0	100	360	RW
-	-	-	-	-
-	-	-	-	-

Access control flag legend:  
R: Read only  
W: Write only  
RW: Read/Write enabled

FIG. 8C

Content of physical memory cell		
Physical address	ID	Logical address
0	10	010:0100
1	21	010:0101
...	...	...
59	33	010:0159
60	2323	016:0000
...	...	...
79	3241	016:0019
80	15	010:0159
...	...	...
83	8	010:0163
...	...	...
360	-589	212:0000
...	...	...
459	-1022	212:0099
...	...	...
...	...	...

FIG. 9B

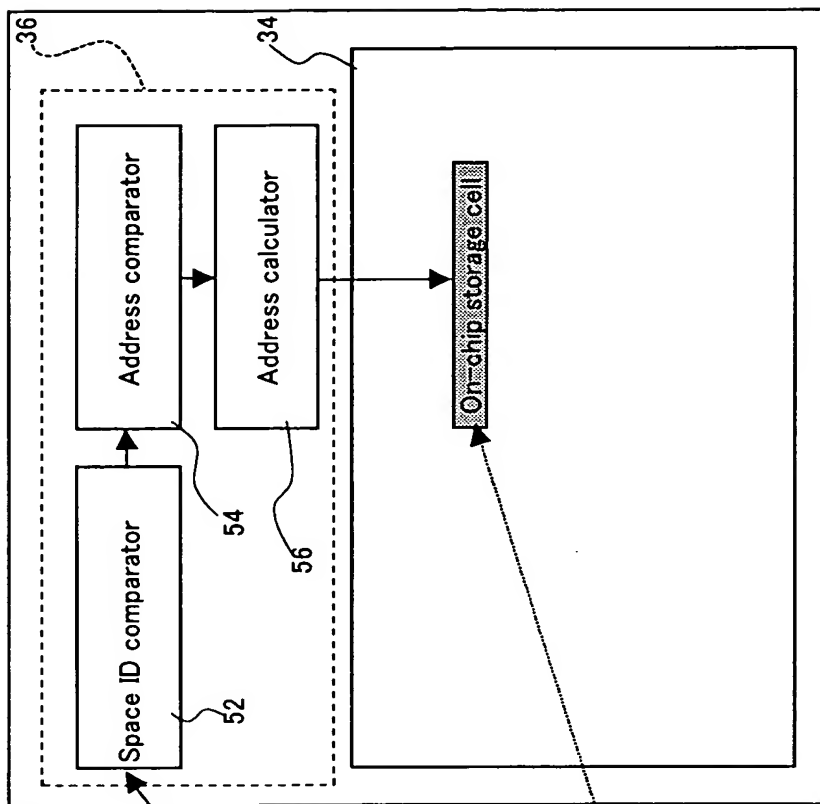


FIG. 9A

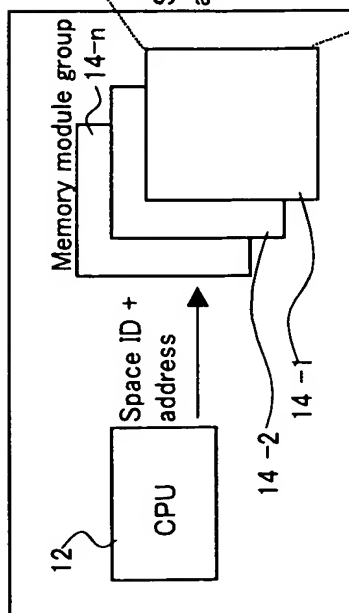


FIG. 9C

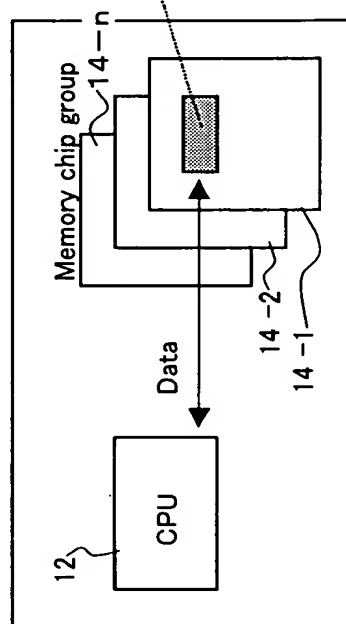


FIG. 10A

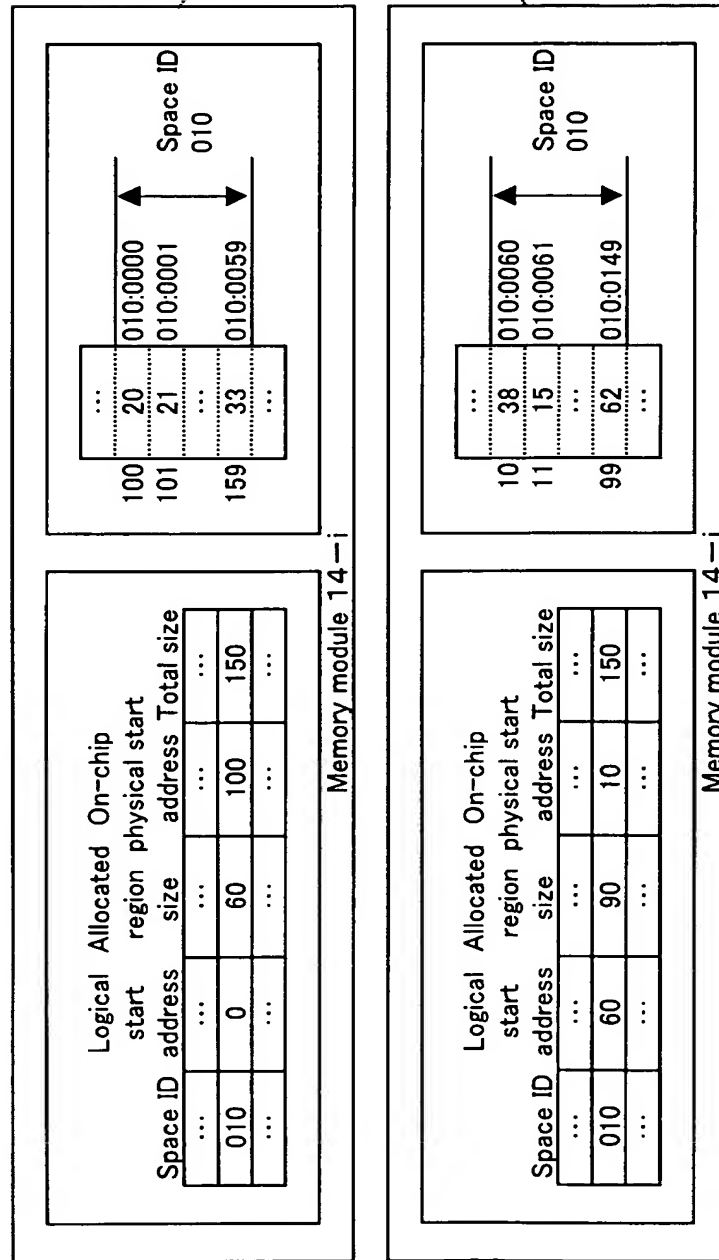


FIG. 10C

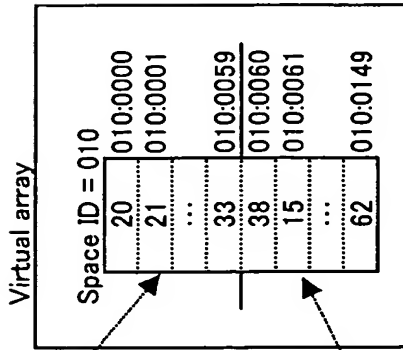
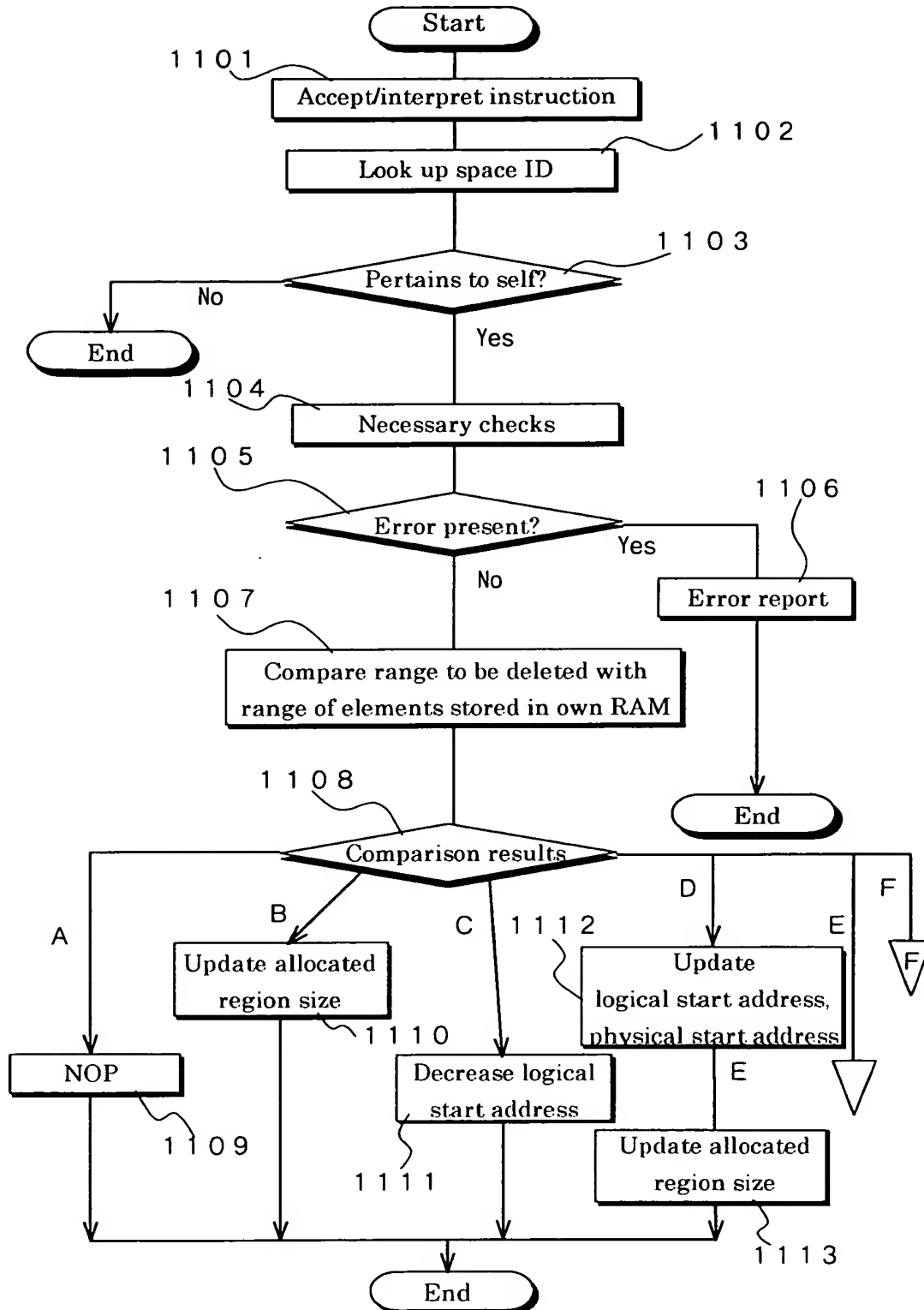


FIG. 10B



9/23

FIG. 11



10/23

FIG. 12A

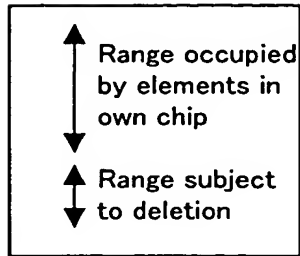


FIG. 12B

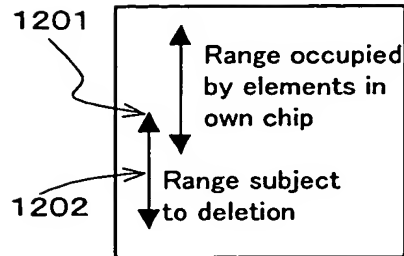


FIG. 12E

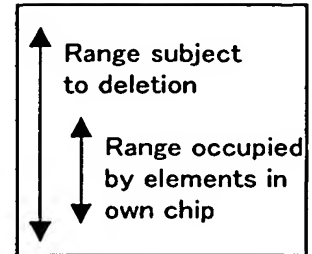


FIG. 12C

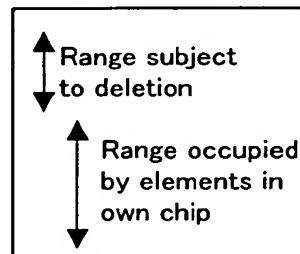


FIG. 12F

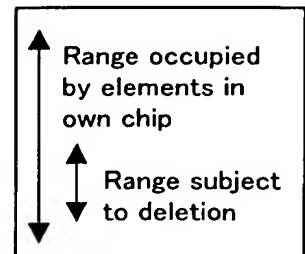


FIG. 12D

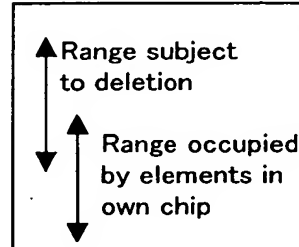
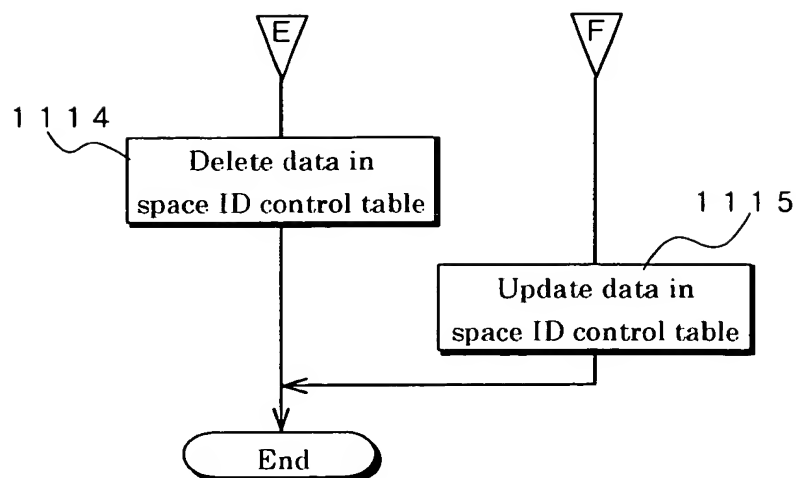
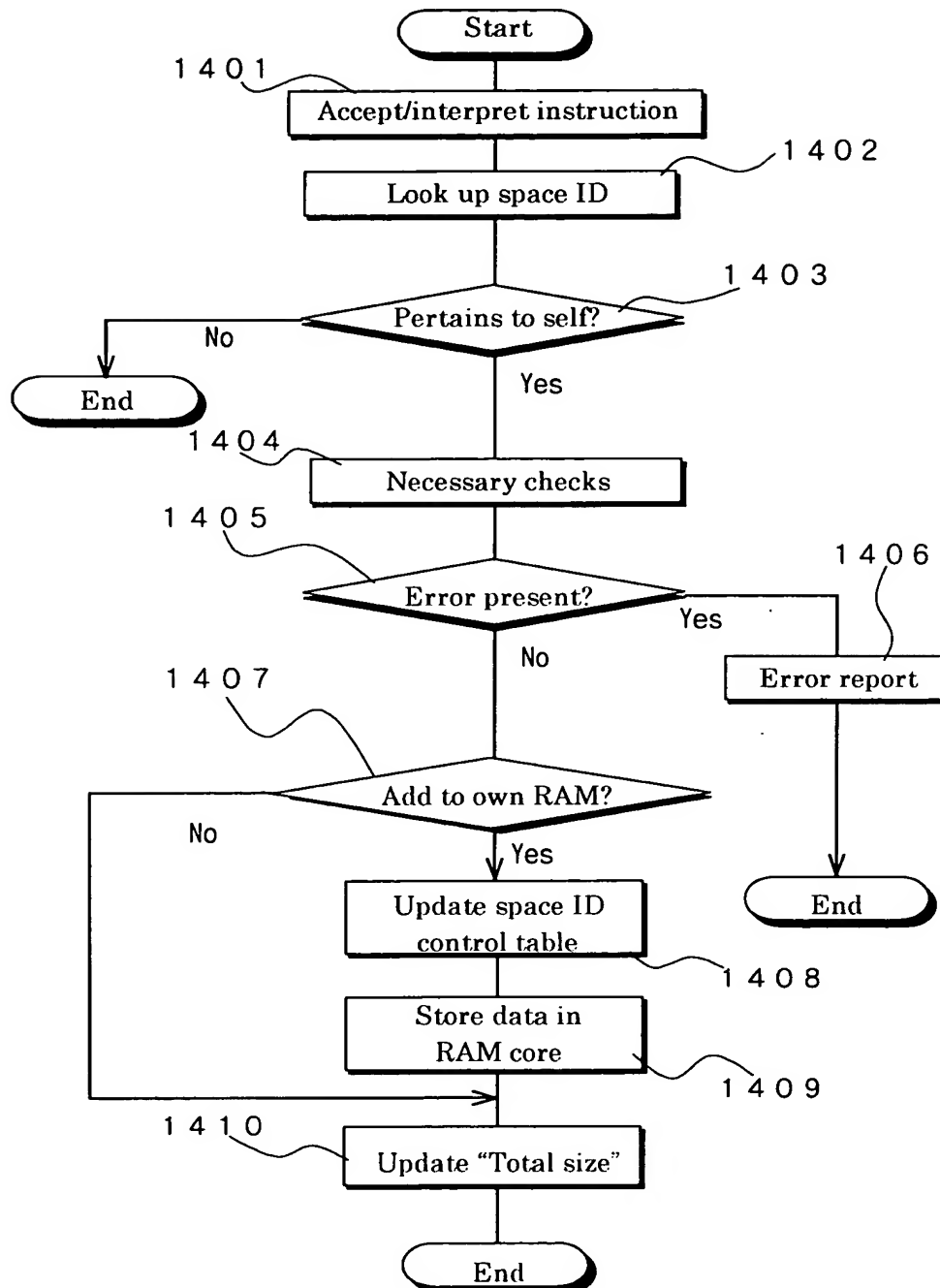


FIG. 13



11/23

FIG. 14



12/23

FIG. 15A

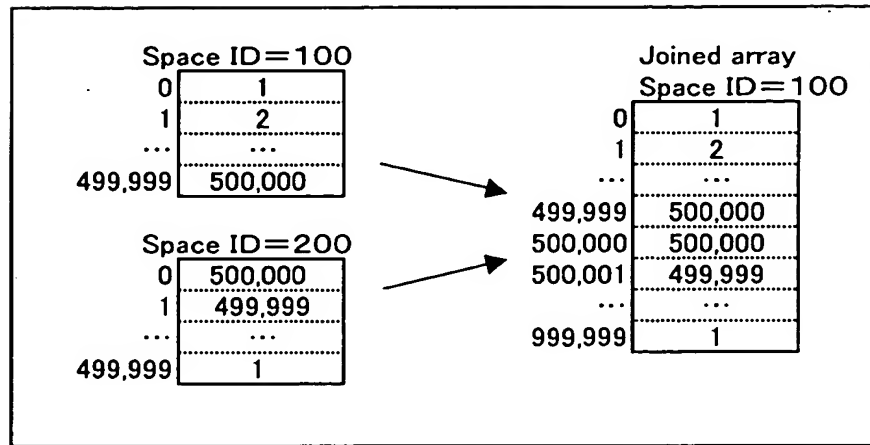


FIG. 15B

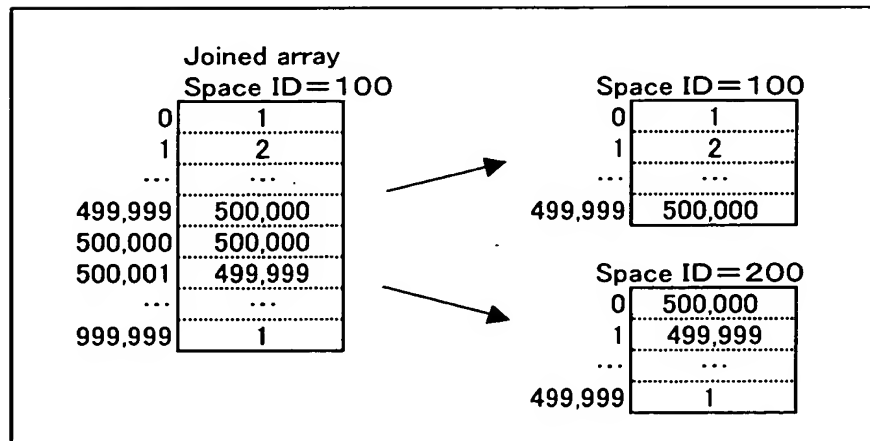


FIG. 16A

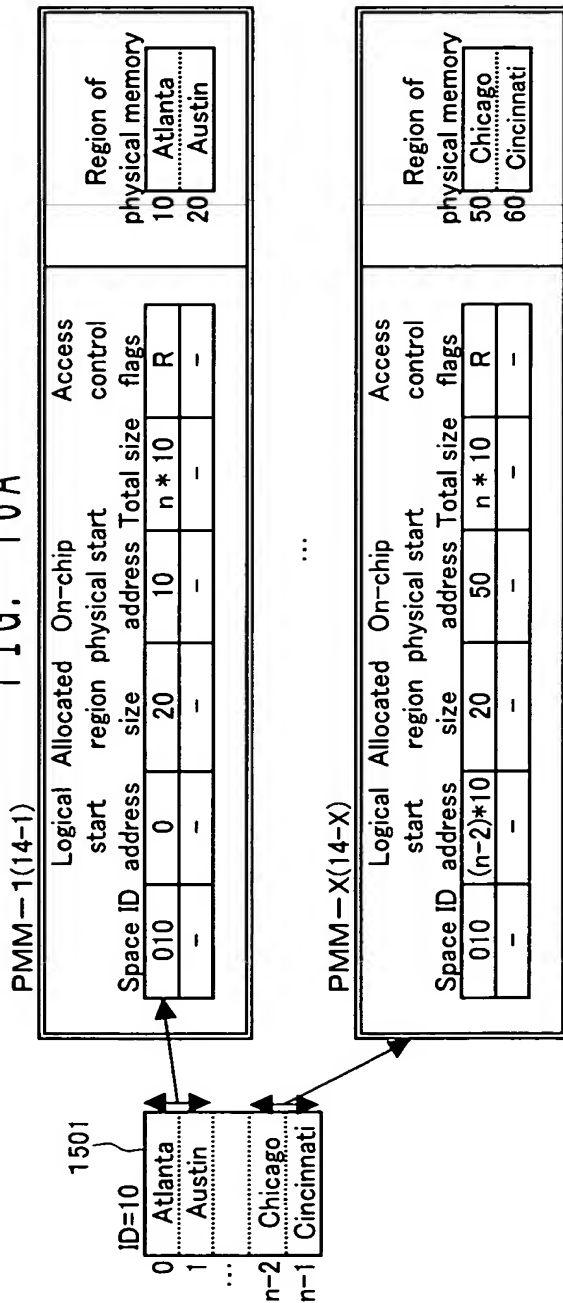


FIG. 16B

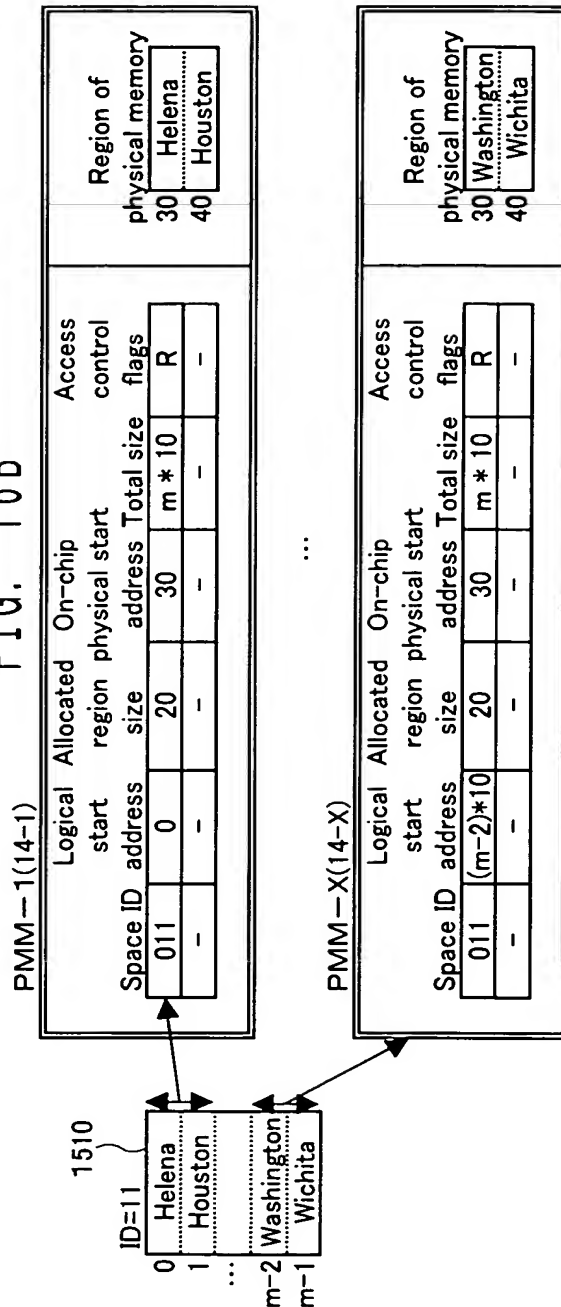


FIG. 17

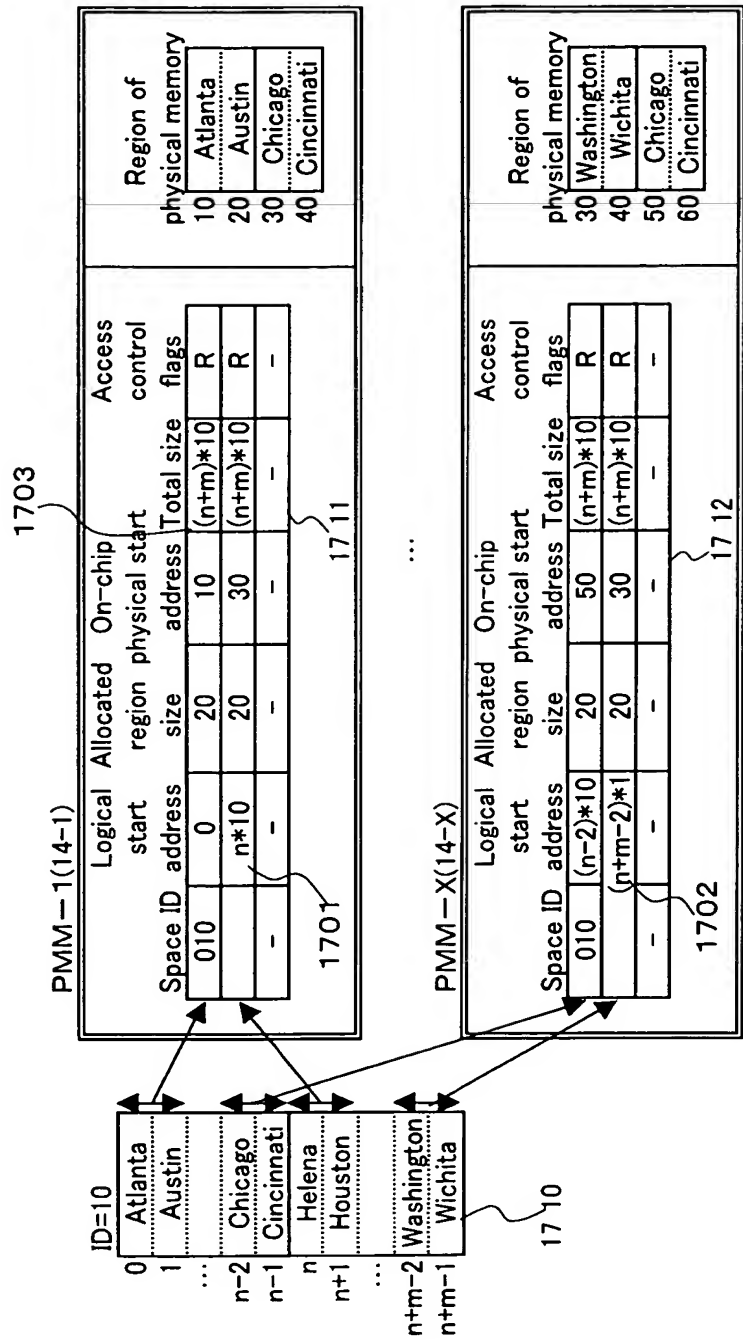


FIG. 18

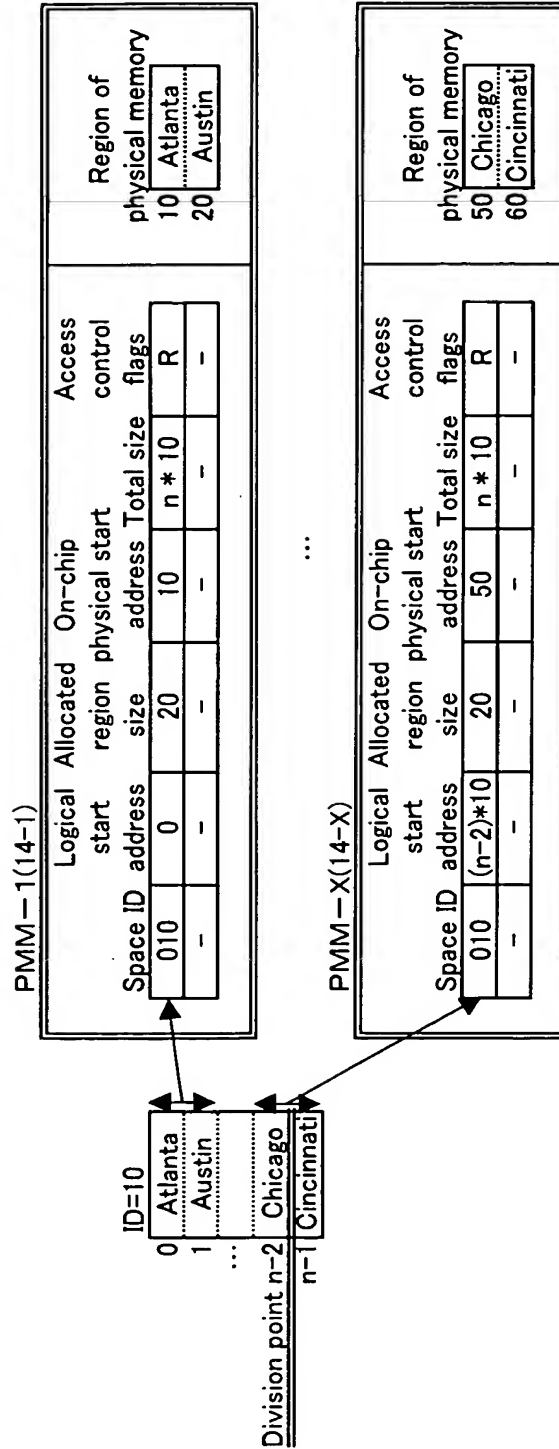
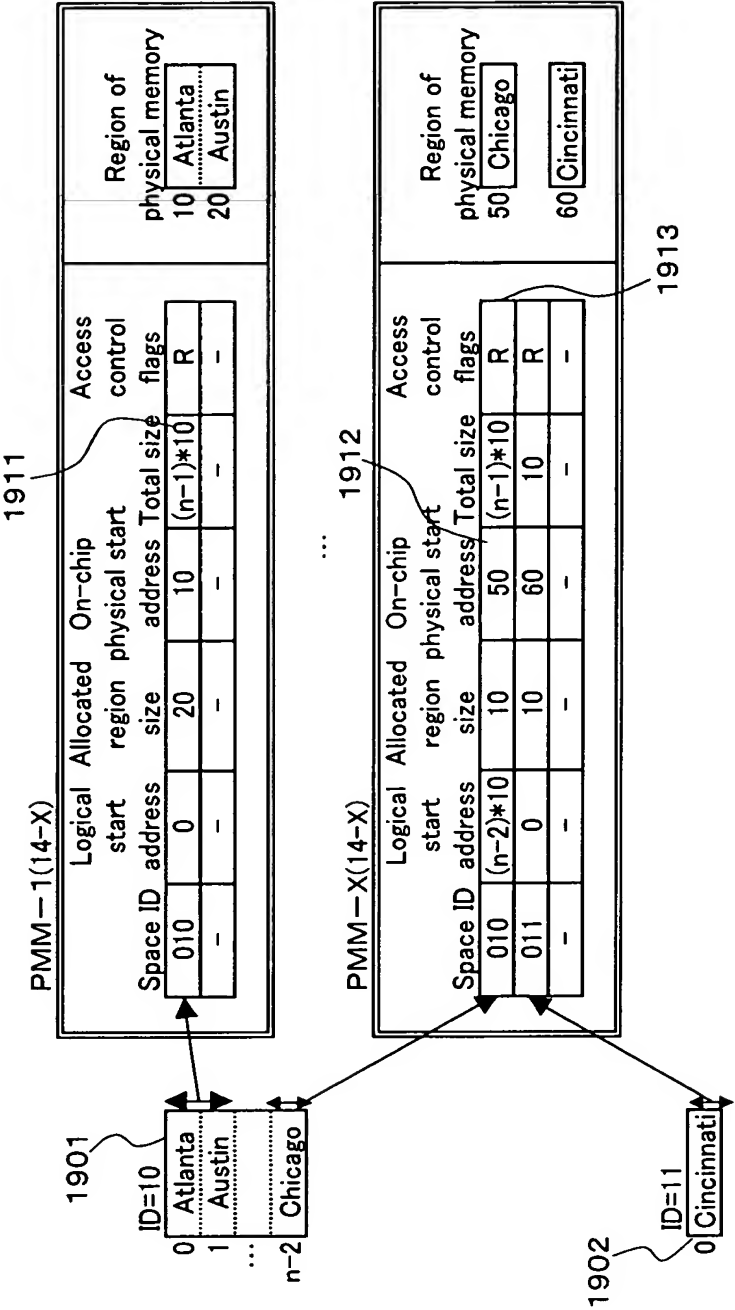


FIG. 19





17/23

FIG. 20

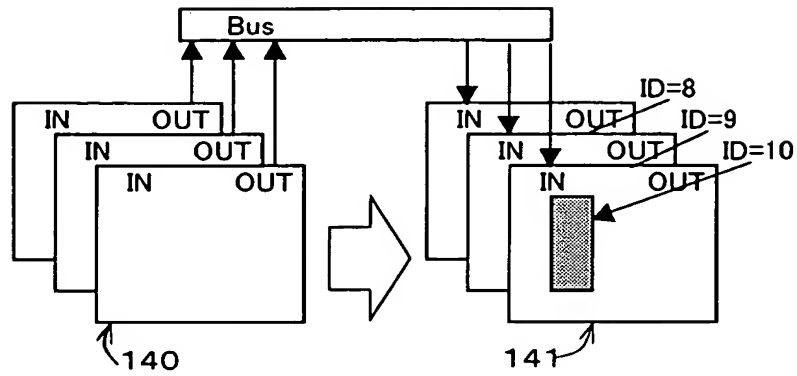


FIG. 21

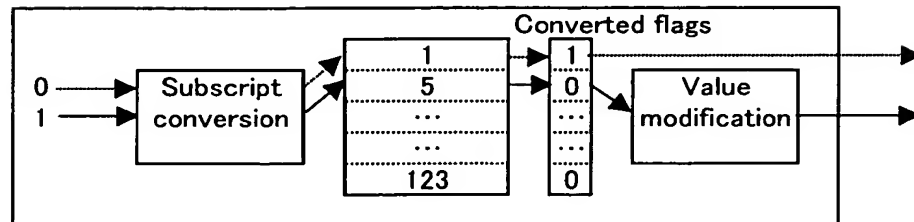


FIG. 22

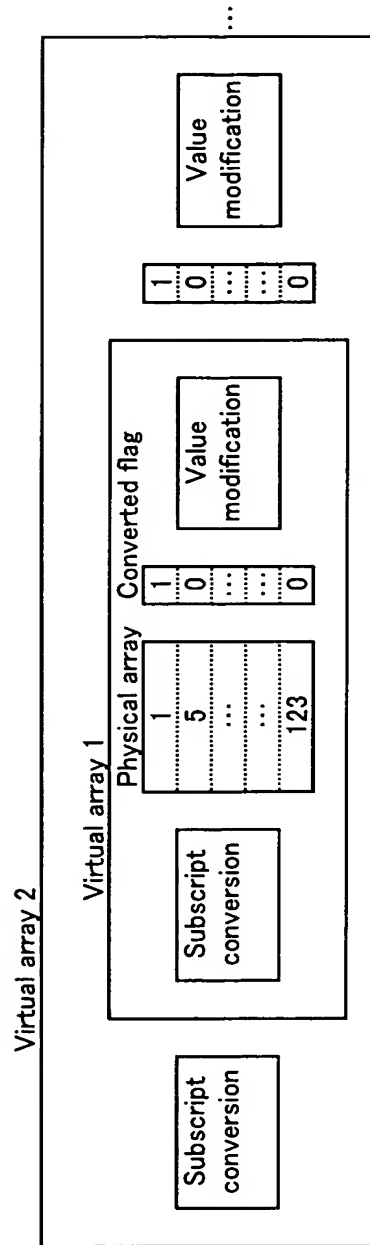


FIG. 23

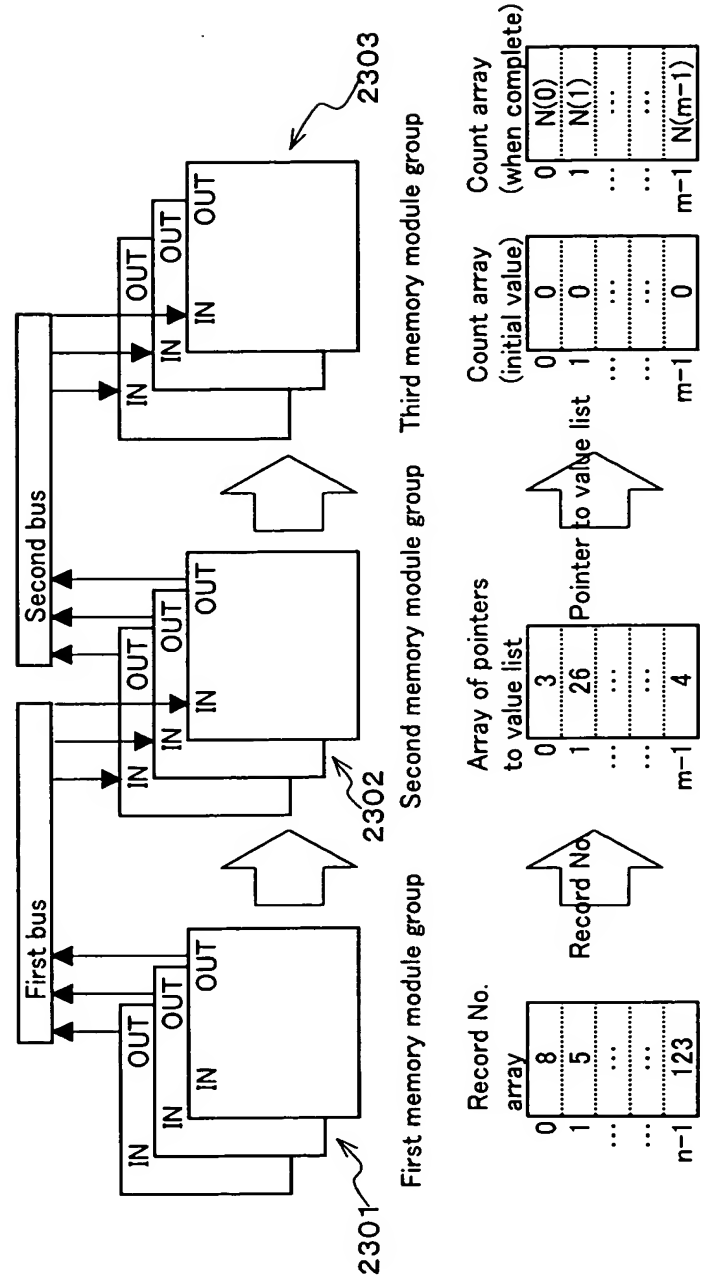
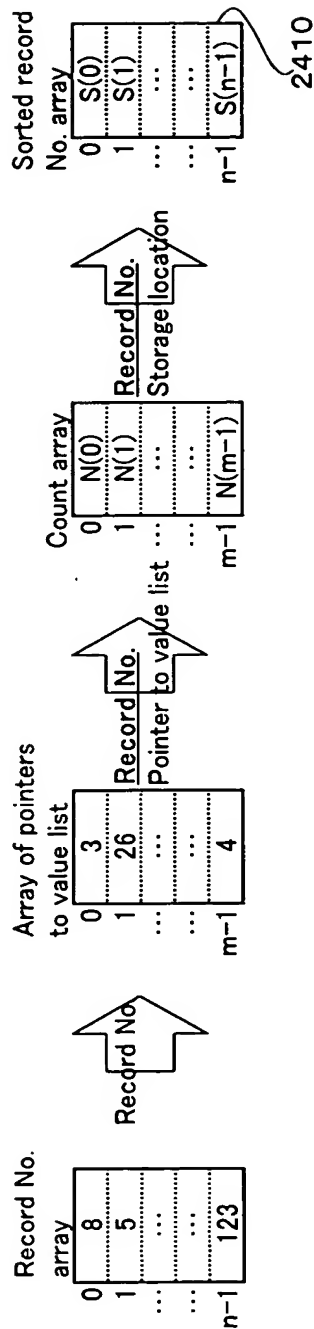
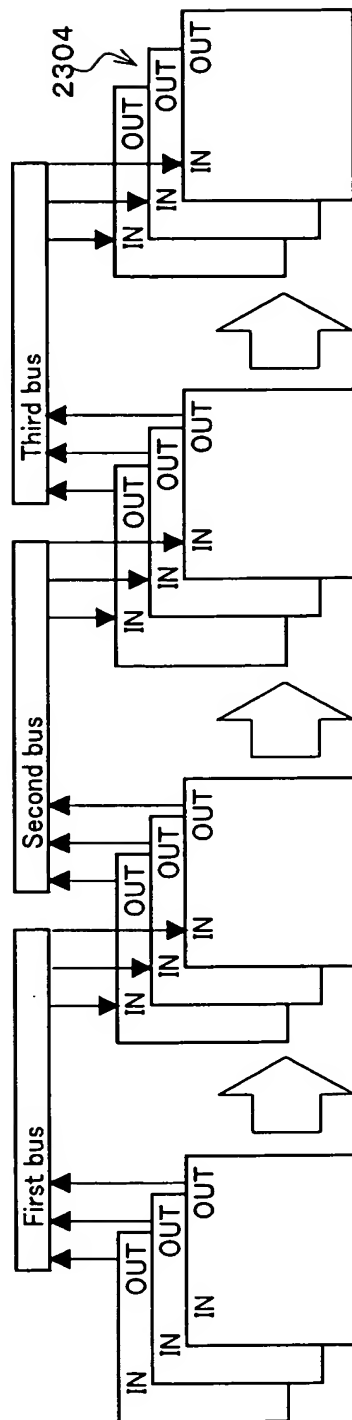


FIG. 24



21/23

FIG. 25

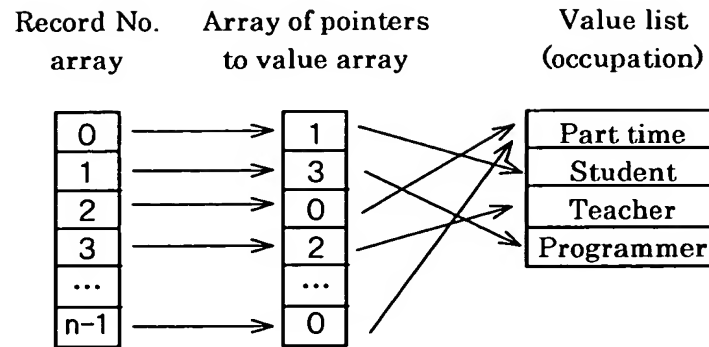


FIG. 27

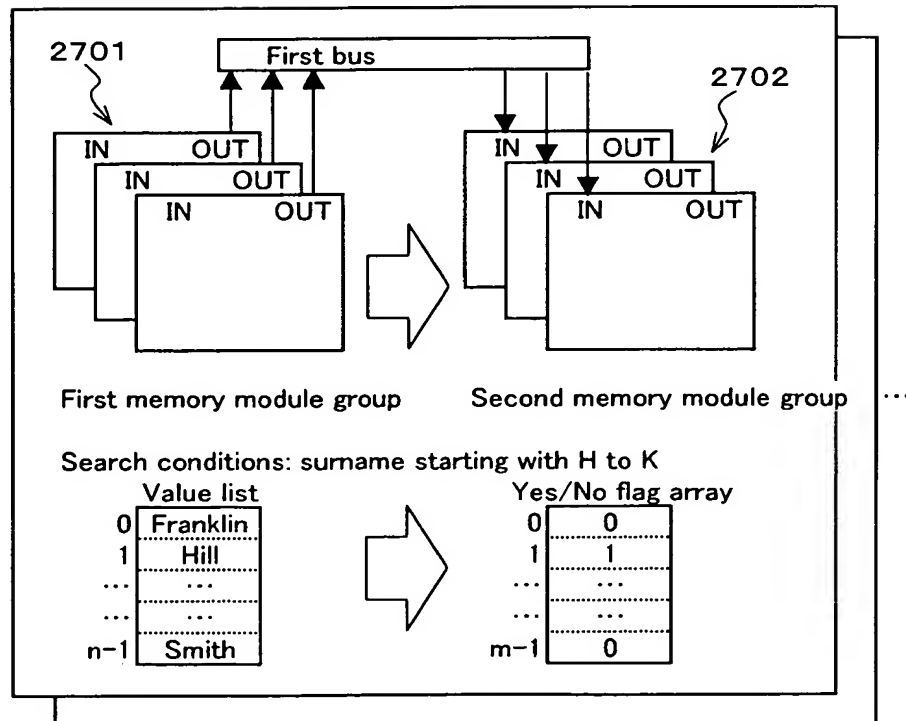


FIG. 26

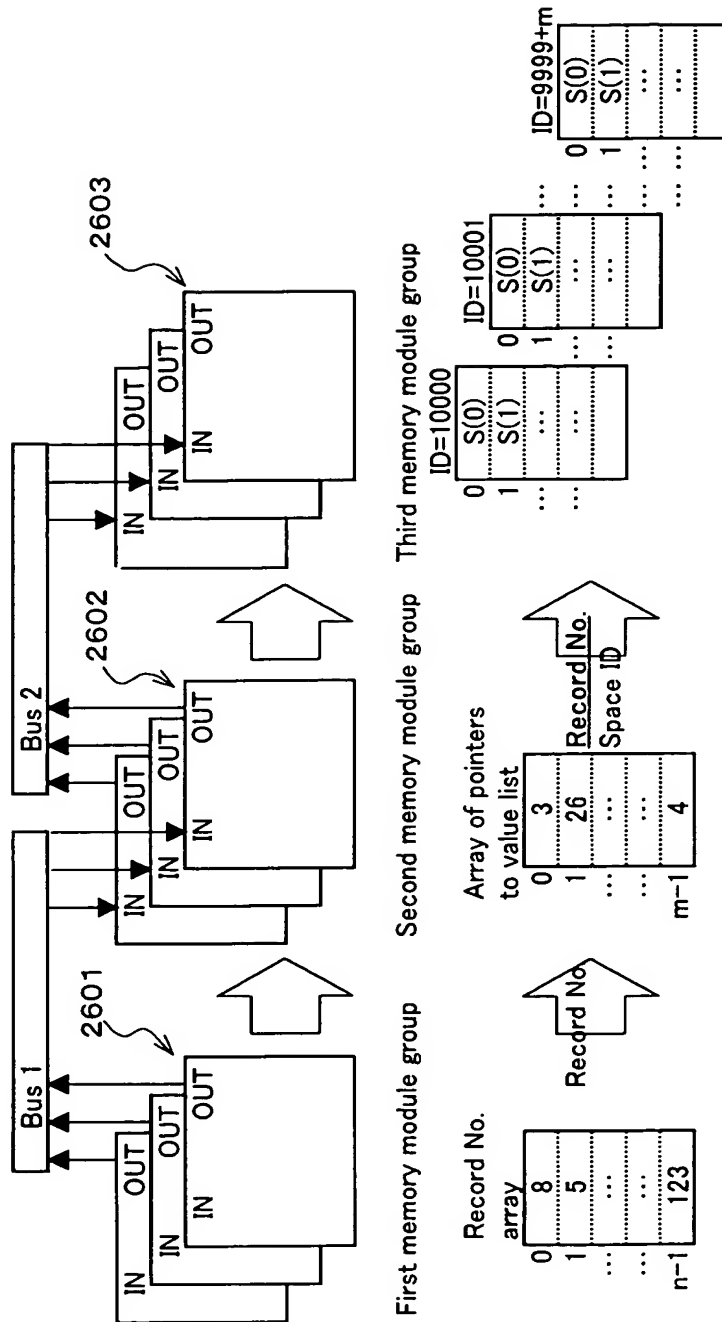


FIG. 28

